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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,200	10/21/2003	Salman Akram	4244.5US (97-1355.05/US)	3680

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,200	AKRAM ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-5 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/21/03, 2/5/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

2. Claims 1-5 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 16-20 of prior U.S. Patent No. 6,383,881 (hereafter '881). This is a double patenting rejection. Note that although the claims are not word-for-word identical, they are considered to be drawn to identical inventions. The word-for-word differences include:

a. In the present application, "the" replaces the usage of "said" in '881, but in each case, the antecedent basis is the same between the application and the '881 patent.

b. Lines 1-3 of '881 include "a method of forming a transistor on a substrate, comprising: forming a dielectric layer on a substrate...", whereas the application states, "a process for making a transistor comprising: providing a substrate; forming a dielectric layer on a portion of the substrate." These statements are considered to be drawn to identical subject matter, because "a method of forming a transistor" and a "process for making a transistor" are literal equivalents. Additionally, the step of "forming a dielectric layer on a substrate" requires the provision of a substrate, so the inclusion of a

step of "providing a substrate" does not in any way limit or change the scope or the subject matter of the claim. Finally, the usage of the word "portion" in line 3 of the application does not limit or redefine the scope of the subject matter of claim 16 in '881, because without further definition as to what constitutes a portion, the word is construed as meaning any area including the entirety of the substrate or any region of smaller area. Similarly, the limitation in claim 16 of '881, which simply states "forming a dielectric layer on a substrate" also would mean forming the dielectric layer over any area including the entirety of the substrate or any regions of smaller area.

The remainder of claims 1-5 of the present application and claims 16-20 of '881 are word-for-word identical. Since the few wording differences between '881 and the present application define exactly identical subject matter and scope, and since it is impossible to infringe upon the rights of either the patent or the claimed subject matter of the application without automatically infringing upon the other, they are considered to be statutory type double patenting.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation of "a gate oxide formed on the dielectric layer." It is not clear as to what is meant by this limitation, since the drawings, specification, and general state of

the art would suggest that the gate oxide layer is formed is formed directly on the substrate, and is actually part of the dielectric layer, rather than being formed on the dielectric layer. For the purposes of examination, it is assumed that the gate oxide layer is formed from the dielectric layer, rather than on top of the dielectric layer, so as to conform with the specification.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,350,665 to Jin et al. (cited by applicant) in view of U.S. Patent No. 6,187,645 to Lin et al. (cited by applicant).

Regarding claim 1, Jin teaches a process for making a transistor, comprising: providing a substrate (402); forming a dielectric layer (figure 4A, above channel 414) on a portion of the substrate (fig. 4A); forming a gate structure having a gate oxide layer formed from the dielectric layer (figure 4A), and a metal silicide layer formed on the gate oxide layer (column 5, lines 37-45), the gate structure having a first and second sidewall (figure 4A; side edges of 404, 406), the sidewalls defining therebetween a first contact region (424-0), a channel region (414) and a second contact region (424-1); and forming first (424-1), second (412-1), and third (fig. 4C, column 8, lines 55-63) within the second contact region (figures 4A-4C), each subregion having a dopant concentration that differs from that of the other two subregions (inherently the case,

since region 424-1 only is doped from process in fig. 4A, and thus is the least heavily doped; central region at 412-1 is doped in the processes of figure 4a, fig 4C, and fig. 4C, and thus is the most heavily doped, and the region between from column 8, lines 55-63 is doped from the processes of figure 4A and figure 4C, and thus has a doping somewhere between the other two). Jin further teaches steps for forming the subregions, comprising: depositing a conformal layer (408; column 8, lines 18-25; see column 2, lines 33-37); anisotropically etching the layer to form a layer of dielectric material on the sidewalls, thus forming single layer sidewall spacers overlying the sidewalls (see column 2, lines 37-42; figure 4B); introducing a first dopant into the substrate to form the first subregion (figure 4A; 424-1); forming another single layer sidewall spacer (410) overlying the single layer sidewall spacer (figure 4B); introducing a second dopant into the substrate to form the second subregion (figure 4B; region 412-1); substantially removing the another single layer sidewall spacer (figure 4C; column 8, lines 55-63); and introducing a third dopant into the substrate to form the third subregion (figure 4C; column 8, lines 55-63).

Jin fails to disclose subjecting the layer of dielectric material on the first and second sidewalls to an annealing/oxidation process.

Lin teaches subjecting the sidewall dielectric spacer to an annealing/oxidation process (see column 4, lines 42-53; figures 3A, 3B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Jin, such that it includes the annealing step suggested by Lin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide the spacer annealing step, because Lin teaches that such a step clears away any crystal

defects on the substrate surface and within the gate structure, which improves the performance of the device (see Lin, column 4, lines 42-53).

Regarding claim 5, Jin teaches that the second single layer sidewall spacer comprises silicon dioxide (column 8, lines 18-25; column 5, lines 45-52).

Regarding claim 2-4, Jin fails to specify spacer thickness values for the embodiment of figure 4.

Lin suggests that the spacer dimensions are selected to minimize gate to drain capacitance (column 1, lines 35-45; column 2, lines 14-24 and to set the length of the LDD region (see figures 1A-C; 3A-E). Lin further teaches that the first spacer thickness is about 150 angstroms (column 3, lines 45-50), and that the second spacers are wider than the first spacers (figures 3A-3E).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the first spacer of Jin is about 150 Angstroms, and the second spacer is significantly wider, as suggested by Lin. The rationale is as follows: A person having ordinary skill in the art would have been motivated to select a first spacer of about 150 angstroms, and a second spacer of 550 angstroms, because doing so enables one to confine the dopant spread in the LDD to areas not under the gate region, and thus prevents undue gate-to-drain capacitance (Lin, column 1, lines 35-45; column 2, lines 14-24). Additionally, selecting a relatively large second spacer thickness allows one to control the distance between the heavily doped drain region and the channel region, thus preventing dopants from the heavily doped regions from migrating to the gate/channel regions (see figures 1 and 3 of Lin). Although neither Lin nor Jin specifically teach the thickness of the second spacer, it has been held that "where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (1955).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,132,757 to Tignor et al. teaches the importance of an anneal/oxidation step in forming an LDD transistor.

b. U.S. Patent No. 6,258,680 and 6,083,846 to Fulford, Jr. et al. teach forming a graded LDD region by sequentially adding or removing spacer layers, followed by an implant step.

c. U.S. Patent No. 5,766,969 to Fulford Jr. et al. discloses forming three doping regions of a drain structure by forming a first spacer, implanting, forming a second spacer, implanting, and then selectively removing the first spacer before the third implant.

d. U.S. Patent No. 6,127,212 to Chen et al. discloses controlling the position of the LDD layer by etching back a first spacer to selected widths.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

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SUPERVISORY PATENT EXAMINER
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